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Metal-Insulator-Metal Diode Process Development for Energy Harvesting Applications

by Matthew Chin, Stephen Kilpatrick, and Dr. Richard Osgood

ARL-TR-5158 **April 2010**

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Metal-Insulator-Metal Diode Process Development for Energy Harvesting Applications

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14. ABSTRACT

Persistent powering of electronics, sensors, and autonomous systems on the battlefield has become increasingly important to the U.S. Army. Scavenging energy from local environments reduces the required energy and weight transported to the theater. Black-body radiation could potentially provide a 24-hr energy source for Army systems. Micro/Nano-scale, metal-insulator-metal (MIM) tunnel diodes will be developed to provide half-wave rectification as part of a "rectenna" energy harvesting system, which includes a radiation-collecting antenna, a rectifying MIM tunnel diode, and a storage capacitor. This research addresses the development, fabrication, and characterization of high frequency MIM tunnel diodes for power rectification. Planar platinum/titanium-dioxide/titanium stacks were fabricated with the focus of determining the effects of the insulator thickness on the electrical performance. Insulator thicknesses were studied between 2 nm and 50 nm. The metals were chosen for their high work function difference, and the insulator was chosen for its barrier height and availability. Metals and insulator thin films were sputtered onto silicon substrates with silicon dioxide overlayers. I-V measurements were taken using an electrical characterization system to confirm a non-linear, asymmetric response.

15. SUBJECT TERMS
MIM diode, rectenna, energy harvesting, rectifier

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1. Background

Methods for extracting or harvesting energy from the surrounding environment are of great interest to the United States Army. With electronics and communications systems becoming increasingly important to the American Soldier for day-to-day operations, energy requirements for powering these systems have grown immensely since their introduction. As it stands, human-portable systems require the Soldier to carry energy in the form of batteries out into the field to keep their electronic systems powered. Batteries account for a substantial percentage of the weight carried by the Soldiers, which in turn leaves less room for food, ammunition, and armor. The purpose of this research is to develop components for a "rectenna" system that would allow electronics to scavenge and harvest energy from the surrounding environment, be it from solar sources, black body radiation, or thermal sources. The components required for such a system include a nano-antenna for radio frequency (RF) energy absorption, a rectifying metal-insulator-metal (MIM) diode for direct current (DC) conversion, and a super-capacitor for energy storage. The focus of this report is on the development of the MIM diode used for rectifying RF energy.

A MIM tunnel diode is composed of two conductive metal layers separated by a very thin dielectric, and operates on the principles of thermionic emission and quantum tunneling (*1*). MIM diodes are desirable for the use in a "rectenna" system due to their ability to rectify at high frequencies (*2*). For the two conductive metal layers, typically two dissimilar metals are used to increase asymmetry between the metal Fermi levels, which improves the nonlinearity of the diode output current. There are many desired properties of a MIM diode used as a rectifier in a rectenna energy harvesting system. A large, nonlinear output current through the diode with respect to a swept voltage across the diode is such a property. The MIM diode should also have a threshold/turn-on voltage that is as small as possible. Using metals with very different work functions, and using a dielectric with a very low barrier height, improves this metric. Additionally, the dielectric material should be as thin as possible while remaining uniform to increase the maximum current output from the device (allowing for more electrons to potentially tunnel through the barrier).

2. Design and Fabrication

The development of a MIM diode suitable for use as a rectifier in a rectenna system is being done in conjunction with Natick Soldier Research Development and Engineering Center (NSRDEC) in Natick, MA. The first step in the development of a MIM diode for rectification was material selection. Several material stacks, including Al-Al_2O_3-Al (*3*), Cr-CrO-Au (*4*), Al-Al_2O_3-Ag (*5*), and Nb-NbO_x-Au (*4*), have been reported to be poor rectifiers due to the large

thermal response when exposed to an infrared (IR) source. Reports have indicated promising results using Ni-NiO-Au and Ni-NiO-Cr (*6*), and as such, collaborators led by Dr. Richard Osgood are currently working on the development of a MIM diode stack using those material systems. The U.S. Army Research Laboratories (ARL) have been working on a novel Ti-TiO2-Pt material system as well as providing fabrication and metrology support to NSRDEC on the Ni-NiO-Au material system.

The Ti-TiO_2-Pt material system was chosen for MIM diode development for the high work function difference between titanium and platinum, for ability to grow a native oxide on titanium, and for titanium dioxide's potentially manageable barrier height (though reportedly higher than the Ni-NiO-Au system). The initial test structure designs for MIM diode fabrication were simple square pillars fabricated on a conductive back-plane (common contact). Measurements are taken on these two-terminal devices by placing a probe on the common, conductive back-plane and a probe on the top metal layer of the pillar, as depicted in figure 1.

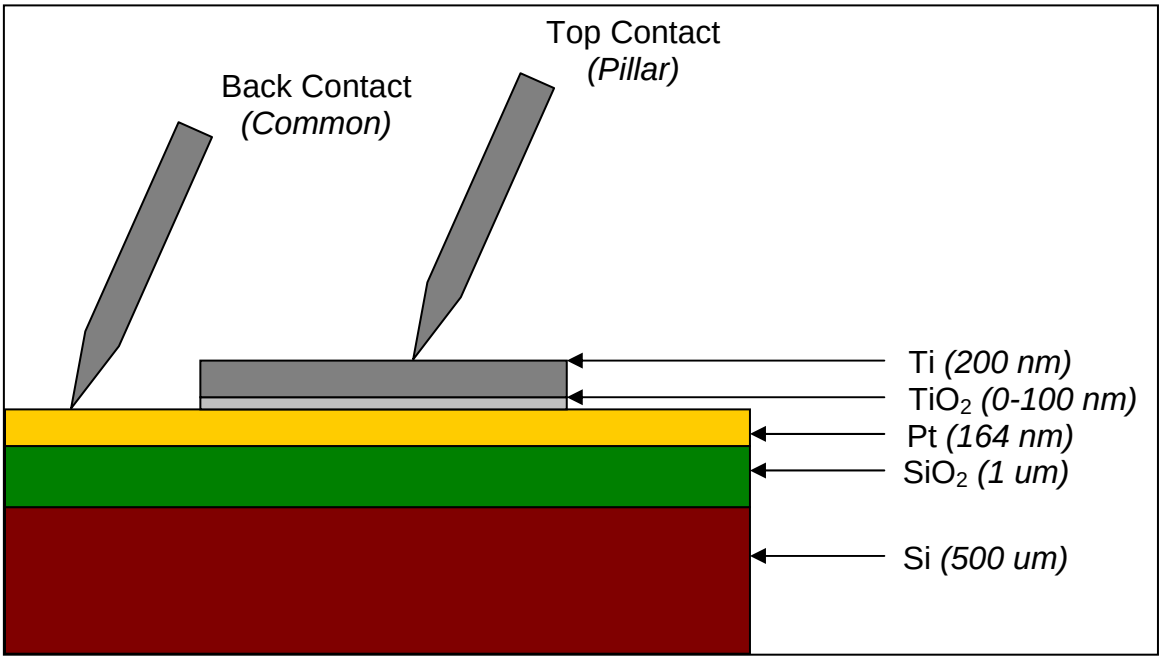

Figure 1. Cross-section of MIM diode material stack and probing locations.

A 4-in silicon wafer with a 1 micron-thick layer of silicon dioxide is used as the substrate for depositing the MIM stack. Platinum is deposited first, followed by the deposition of titanium dioxide and titanium. Although the design is crude, it allows for the deposition of the entire MIM material stack to be done without breaking the vacuum within a multi-material system DC sputtering tool. A CAD layout of a MIM pillar patterned die is shown in figure 2. A detailed process flow is provided in table 1 and example values of actual process runs are given in appendix A.

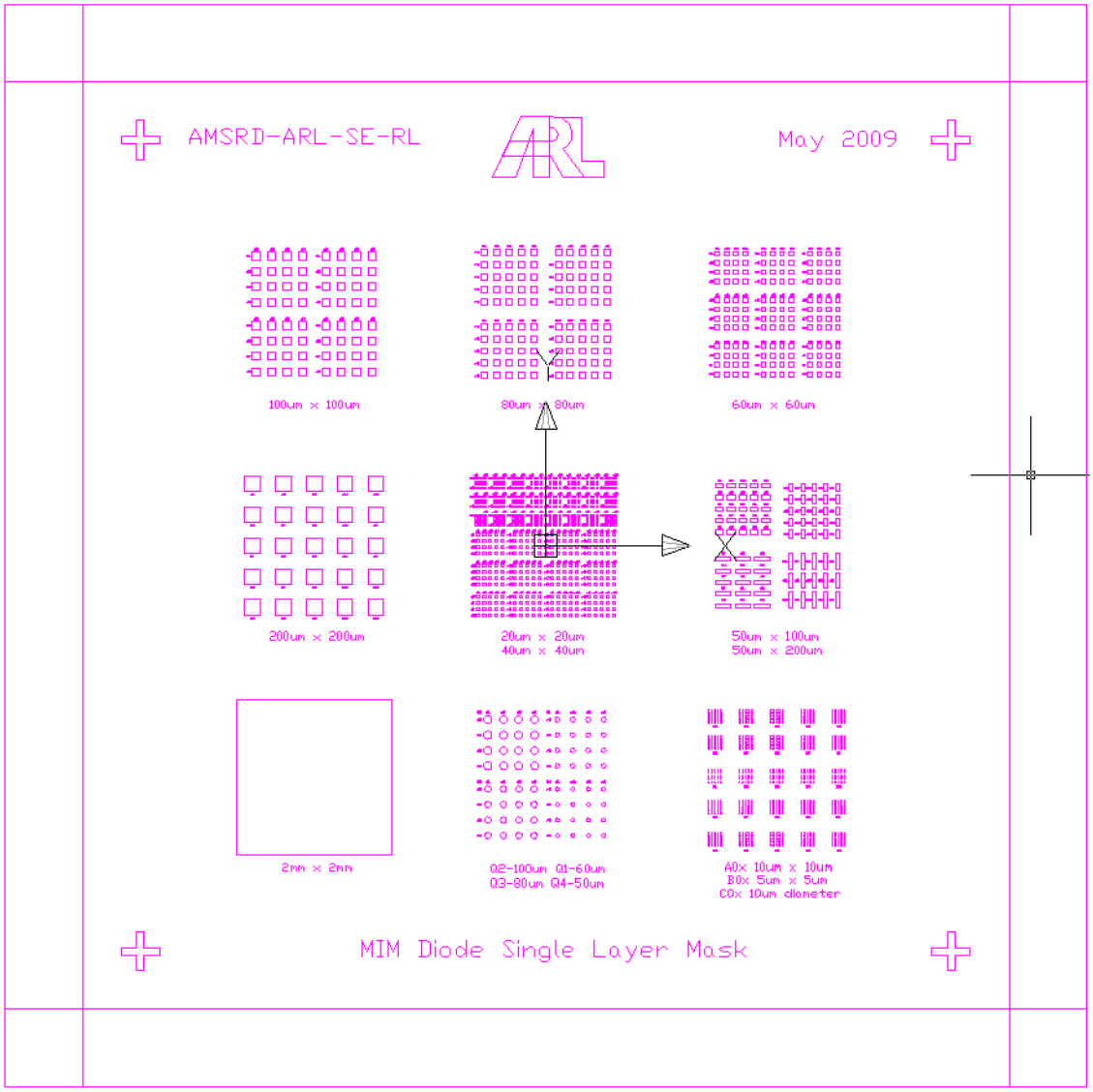

Figure 2. The MIM diode mask provides the patterning for 18 different pillar sizes and geometries ranging from a 2 mm x 2 mm square, to as small as 5 µm x 5 µm squares and 10 µm diameter circles.

Table 1. Process flow description for the fabrication of a MIM diode.

1	Substrate Cleaning	The Si/SiO_2 substrate is cleaned using an acetone, isopropyl alcohol, and deionized water rinse, followed by a nitrogen dry and soft-bake to remove any moisture from the surface.
2	MIM Stack Deposition	A multi-material sputtering system is used to deposit Pt, TiO_2, and Ti without breaking vacuum. The Pt and Ti are deposited using DC sputtering, while the TiO_2 is deposited using a reactive sputtering in oxygen plasma. Future iterations added a 10-min annealing step in the presence of O_2 to allow for the TiO_2 to uniformly form.
3	Surface Cleaning	After the MIM blanket deposition, the surface is cleaned using an acetone, isopropyl alcohol, and deionized water rinse, followed by a nitrogen dry. The wafer is then placed on a hotplate for 3–5 min to allow all moisture to evaporate.
4	Spin On Resist	AZ 5214 reverse image photoresist is spun on to pattern the MIM pillar patterns on the wafer. The resist is then soft-baked to firm up the resist.
5	Photolithography	The wafer with photoresist is placed on an aligner where the MIM diode mask is used to lay down the pattern. The wafer is then exposed to UV light.
6	Development	The exposed wafer is developed, using the development solution to remove photoresist where it was exposed to the UV light, leaving only the MIM diode patterns.
7	Surface Cleaning	The surface of the wafer is cleaned to remove any developer or resist residue in the patterned areas by using a very light ashing (descum) recipe in oxygen plasma.
8	Edge Bead Removal	Acetone is used to clean the edges of the wafers before the photoresist curing/hardening step to avoid flaking and residue build-up on the wafer edges.
9	UV Curing	The photoresist on the wafer is cured at higher temperatures (around 220 °C) using UV light for a long period of time. This hardens the resist so that it may withstand the ion milling process.
10	Ion Milling	An anisotropic dry etch is performed on the wafer to remove the top metal layer and the insulator layer around the pillar structures, leaving the bottom metal layer exposed. The hardened resist protects the pillar areas, while all areas are etched away.
11	Photoresist Removal	After the dry etch leaves the desired diode patterns, the photoresist is removed using an ashing process in oxygen plasma. Care must be taken to not run the oxygen plasma too long due to the presence of titanium metal, which can easily oxidize in such an environment if care is not taken.
12	Inspection and Dicing	The final wafer is inspected and then diced into individual die using a wafer scribe. The individual dies are then measured on a probe station for electrical parameters.

During the initial fabrication run, we fabricated four wafers with approximately 20 die being produced from each wafer. Physical images of portions of the die are shown in figure 3. It should be noted that although the process flow shown in table 1 was used for three of the wafers, the first wafer fabricated used a very different process involving a lift-off process rather than an ion milling process. This wafer also had a gold back-plane rather than using the bottom layer of

the MIM diode stack to act as the conductive, common back-plane. There were fabrication issues that prompted the change from a lift-off process to an ion milling process, mainly concerning the titanium oxide growth. The heat required to properly produce the titanium oxide layer could not be achieved with a lift-off process flow, due to the presence of photoresist that could not be heated to those temperatures.

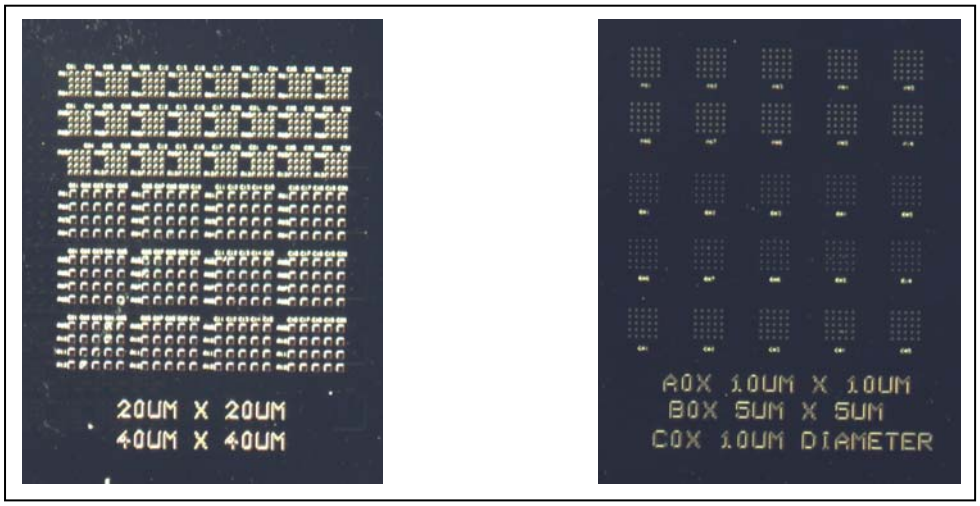

Figure 3. Optical microscopy images of pillar blocks on a MIM diode die. Both circular and square pillars were fabricated. Represented in the images above include the 40 µm x 40 µm, 20 µm x 20 µm, 10 µm x 10 µm, 5 µm x 5 µm, and the 10 µm diameter pillars.

We recognized that the titanium oxide layer would potentially prove to be a difficult layer to control, due to inherent uniformity issues and its thin thickness. Three of the wafers that we fabricated were used to test various titanium dioxide thickness recipes, which included a control of 0 nm of TiO_2, one wafer with 2 nm of TiO_2, and the one wafer with 4 nm of TiO_2. All recipes involved made use of a reactive sputter process involving a Ti target and oxygen plasma to produce the insulator. We kept the temperature and gas flow ratios constant, while only the deposition time was varied (in the case of the control, the deposition time was 0 s).

3. Experimental Setup and Measurements

Eighty-two devices from four different wafers were electrically measured using a Micromanipulator probe station and a Keithley 4200 Semiconductor Characterization System. All four wafers were measured using the same settings and equipment. Two-terminal I-V characteristics were measured with voltages swept in both the positive and negative directions over two sets of ranges. Ideally, the I-V curves from these MIM diodes would have a non-linear "kink" located where no applied voltage (i.e., 0 V) with a near-zero current produced in the negative applied voltage region, and an exponential current gain produced in the positive applied

voltage region. The measurement settings used for the taking the two-terminal I-V characteristics of the fabricated MIM diodes are shown in table 2. Additional setting information used can be found in appendix B (all details for replicating this measurement can be found).

Table 2. MIM diode measurement settings for the Keithley 4200 SCS.

I-V Sweep (–0.2 mV to 0.2 mV)		**I-V Sweep (–2 mV to 2 mV)**	
Voltage Start Value:	–0.2 mV	Voltage Start Value:	–2 mV
Voltage Stop Value:	0.2 mV	Voltage Stop Value:	2 mV
Voltage Step Value:	0.002 mV	Voltage Step Value:	0.02 mV
Reverse V Sweep:	Yes (same range)	Reverse V Sweep:	Yes (same range)
Data Points:	201	Data Points:	201

I-V characteristics were similar for all four wafers tested in both I-V sweep ranges. Some typical output graphs are shown in figures 4 and 5, representing the –2 mV to 2 mV sweep and the –0.2 mV to 0.2 mV sweep, respectively.

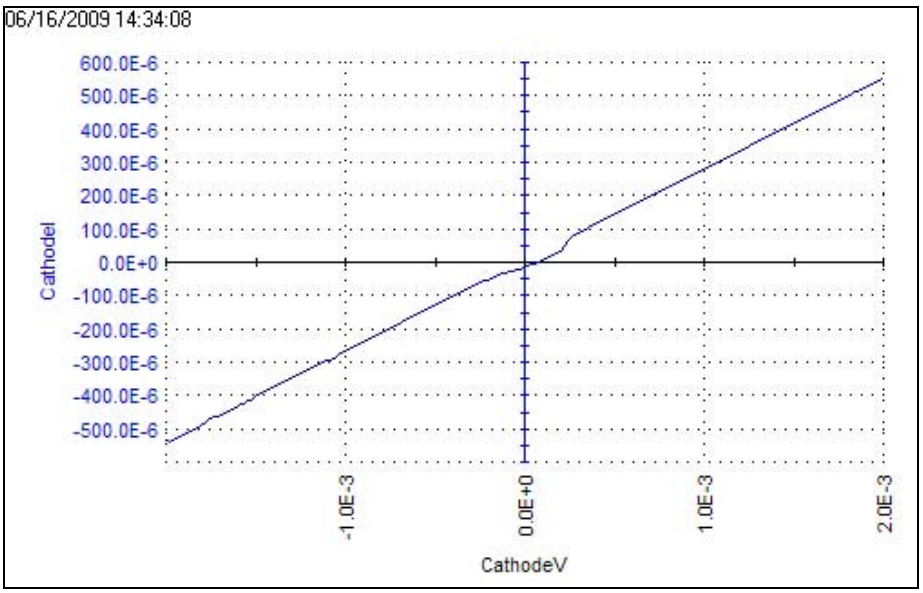

Figure 4. Output current with respect to an applied voltage sweep ranging from –2 mV to +2 mV. Please note that the kink between –0.2 mV and 0.4 mV is due to a measurement artifact on the system and is not a real portion of the signal (it is actually linear through that region, confirmed by additional measurements).

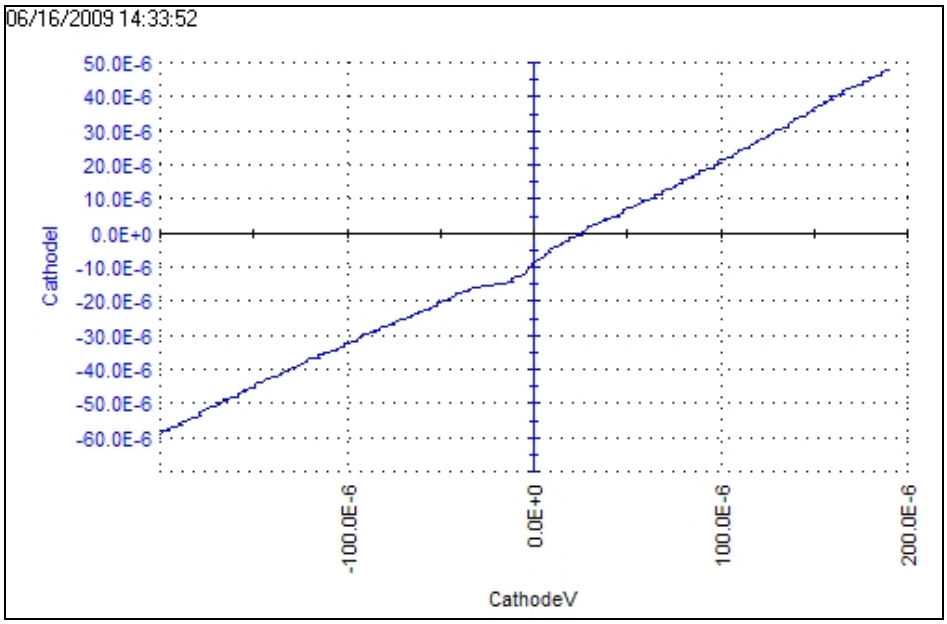

Figure 5. Output current with respect to an applied voltage sweep ranging from –0.2 mV to +0.2 mV. Please note that the kink between –0.03 mV and 0.3 mV is due to a measurement artifact on the system and is not a real portion of the signal (it is actually linear through that region, confirmed by additional measurements).

As stated previously, one wafer was fabricated differently using a lift-off process rather than the ion milling process, but was made using the same MIM diode pattern mask. The three wafers that were fabricated using the ion milling process were made with recipes varying the titanium dioxide thickness (0 nm, 20 nm, and 40 nm). Devices that were measured include various devices from each of these four wafers. In addition to the variations of oxide thickness, on each die exists multiple pillar geometries. We measure devices that came from one of three pillar geometries, including 200 µm x 200 µm squares, 100 µm x 100 µm squares, and 80 µm x 80 µm squares. The primary reason why these three pillar geometries were chosen was for their ease of probing on the measurement apparatus. Due to the probe size and the requirement of scratching into the material for an adequate contact, these three larger sizes were found to be the most appropriate devices to measure for the initial measurement runs. Data (I-V sweeps) were collected and broken down into the following categories:

Insulator (TiO_2) Thickness:

- 0 nm
- 20 nm
- 40 nm

Pillar Geometry:

- 200 µm x 200 µm

- 100 µm x 100 µm
- 80 µm x 80 µm

4. Results and Discussion

From the data collected, there were a few trends that we picked out immediately. The linear curvature presented in the I-V characteristics of figures 4 and 5 is common in every single one of the 82 devices measured across the four wafers and the three pillar geometries. The high linearity of the I-V characteristics for all of the MIM diodes indicates that none of the devices function as diodes, but rather, poor resistive elements. Using Ohm's Law, the inverse of the I-V slope can be used to crudely calculate a rough resistance (in ohms) of the device. Since all devices measured appear to be operating as resistors, the resistance of the devices was used as a figure-of-merit to compile the data in a statistical summary, as shown in tables 3 and 4. Figures 6 and 7 provide some representative graphs of each table, emphasizing how similar the results are, regardless of titanium dioxide thickness or the pillar geometry.

Table 3. Statistical summary for MIM diodes with respect to insulator thickness.

	0 nm TiO_2	**20 nm TiO_2**	**40 nm TiO_2**	**All Devices**
Devices Measured	11	59	12	82
Minimum Resistance	3.23 ohms	3.33 ohms	3.15 ohms	3.15 ohms
Maximum Resistance	3.65 ohms	9.90 ohms	4.58 ohms	9.90 ohms
Median Resistance	3.43 ohms	6.25 ohms	3.48 ohms	5.33 ohms
Average Resistance	3.44 ohms	6.28 ohms	3.54 ohms	5.50 ohms
Standard Deviation	0.140 ohms	1.69 ohms	0.381 ohms	1.91 ohms

Table 4. Statistical summary for MIM diodes with respect to pillar geometry.

	80 x 80 µm	**100 x 100 µm**	**200 x 200 µm**	**All Devices**
Devices Measured	31	29	22	82
Minimum Resistance	3.15 ohms	3.17 ohms	3.29 ohms	3.15 ohms
Maximum Resistance	9.90 ohms	9.01 ohms	7.86 ohms	9.90 ohms
Median Resistance	5.90 ohms	5.77 ohms	3.73 ohms	5.33 ohms
Average Resistance	5.97 ohms	5.62 ohms	4.66 ohms	5.50 ohms
Standard Deviation	2.10 ohms	1.85 ohms	1.49 ohms	1.91 ohms

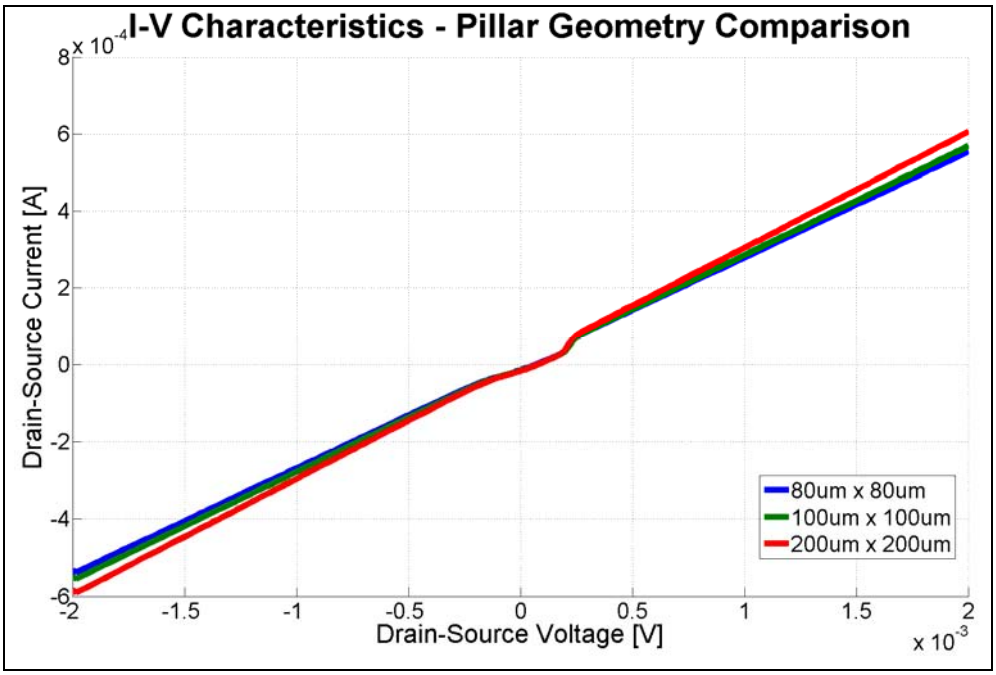

Figure 6. Comparison of representative I-V curves for different pillar geometries.

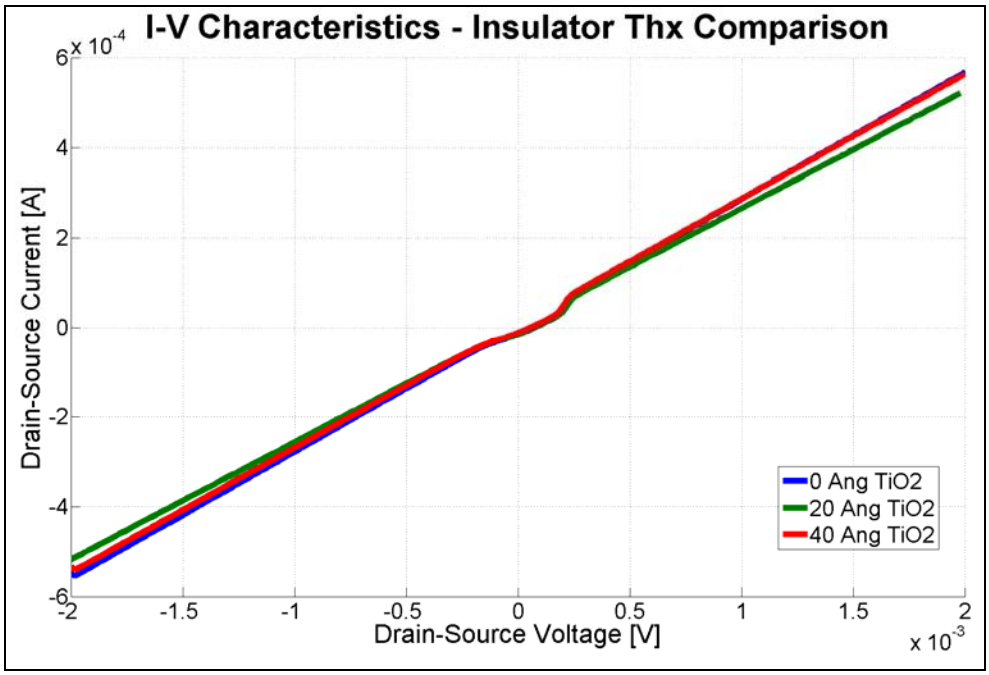

Figure 7. Comparison of representative I-V curves for different oxide thicknesses.

From the summaries, it can be seen that nearly all of the devices measured possess a calculated resistance (derived from the slope of its measured I-V curve) between 3 ohms and 9 ohms. These resistance values are extremely low, with much of that resistance potentially being attributed to the contact resistance of the probes. More disconcerting is the fact that the results

were very similar regardless of the titanium oxide thickness (note that the increase of variability in the 20 nm thickness data can be attributed to the substantially larger sample set and that data was taken from two wafers compared to one wafer for the 0 nm and 40 nm thicknesses). This indicates that either the titanium dioxide insulating layer is not properly forming during the fabrication process (in this case, reactively sputtering Ti in oxygen plasma), or that the dielectric is so thin, too many electrons are able to tunnel through the barrier. In all probability, the lack of a thin, uniform layer of titanium dioxide is the reason for the poor results and no evidence of diode action in the I-V characteristics. Pin-holing, islanding, and incomplete oxidation of titanium are all known issues with reactively sputtering thin dielectrics from a metallic source. Methods to potentially rectify these issues are discussed in the next section.

5. Next Steps and Current Progress

The conclusion that we drew from the current data is quite simple: the MIM diodes are not diodes, but rather extremely poor resistive elements. This can be seen straight from the I-V characteristics collected from the 82 measured devices. Non-linear behavior is nowhere to be seen in the current set of fabricated devices. This means that something must be corrected in the fabrication process, and that the culprit of these poor results lies somewhere with the insulating layer of the devices.

Efforts have already been started to rectify this issue in the fabrication of the dielectric layer. We have suspected that the reactively sputtered titanium is not fully oxidizing before it deposits on the wafer, creating shorts between the metal layers of the MIM diode. A potential solution to this issue is to expose the deposited titanium dioxide layer to a short anneal in an oxygen atmosphere, allowing it to react to any titanium left in the layer that had not reacted up to that point. Issues with pinholes and islands will be more difficult to overcome, but they can be ruled out if a relatively thick titanium dioxide layer is grown.

An optimized titanium dioxide deposition recipe will be needed to create reliable Pt-TiO_2-Ti MIM diodes in the future for use in rectenna systems. A design-of-experiment (DOE) is currently underway to determine the best temperature, gas flow ratio, and time (directly associated with thickness) to sputter the titanium dioxide insulating layer for extremely thin films. This DOE is currently being performed for the Unaxis Clusterline Sputter System. With guidance from the field engineer of the system, values were chosen for the three variables to be reviewed in the DOE. Appendix C provides both details and justification for the variables explored in the DOE, as well as a table of experiments that are in progress or that will be performed.

While a functional MIM diode for power rectification in a rectenna system has yet to be achieved, there are still many avenues of exploration still yet to be reviewed and much work that

still needs to be done. Immediate objectives include ongoing work with creating a reliable, uniform dielectric in the Pt-TiO_2-Ti material system, as well as developing better MIM diode designs to allow for smaller diode areas that are still capable of being probed. NSRDEC has shown great potential with the Ni-NiO-Au material system, with the achievement of a non-linear device, and hopefully, ARL is not too far behind in confirming the usefulness of a TiO_2-based MIM diode.

6. References

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Appendix A. MIM Diode Process Flow Example Run

Project Name:	Metal-Insulator-Metal Diode Project (Component of Rectenna)
Experiment Name:	Titanium Dioxide Recipe and Process Development
Entry Type:	Fabrication
Entry Page Span:	3 pages

Wafer ID:	**W21 (TiO_2 @ 500 °C for 1923 s in 20 sccm/20 sccm Ar/O_2)**	
	W09 (TiO_2 @ 300 °C for 1923 s in 20 sccm/20 sccm Ar/O_2)	
	W27A (TiO_2 @ 500 °C for 1923 s in 30 sccm/10 sccm Ar/O_2)	
Wafer Start:	07/24/2009	
	Substrate Type:	4-inch Si
	Substrate Thickness:	unknown thickness
	Other Info:	1 um of SiO_2 present
Cleaning:	07/27/2009	
	Solution(s):	Acetone/IPA/De-mineralized water rinse
	Post Process:	Nitrogen dry
	Soft Bake:	110°C for 60 s
Stack Deposition:	(ALL – various dates 07/2009)	
	Process Tool:	CLC 200 Unaxis Clusterline Sputter Tool
	Dep Method:	Sputtering (DC Magnetron)
	Recipe:	MC_Pt 1640A_TiO2 1000A_Ti 2000A_500C_1a
		MC_Pt 1640A_TiO2 1000A_Ti 2000A_300C_1a
		MC_Pt 1640A_TiO2 1000A_Ti 2000A_500C_2
	Base Pressure:	~2-3x10^{-4} mbar
	Base Power:	1000W
	M1 Material:	Titanium
	M1 Temp:	500°C
	M1 Dep Time:	18 s
	M1 Gas Flow:	30 sccm Ar
	M2 Material:	Platinum
	M2 Temp:	500°C
	M2 Dep Time:	
	M2 Gas Flow:	20 sccm/ 20 sccm O_2/Ar for W09/W21(X3)
		10 sccm/ 30 sccm O_2/Ar for W25A(22)
	I Material:	Titanium Dioxide
	I Temp:	500°C
	I Dep Time:	1923 s
	I Gas Flow:	20 sccm/ 20 sccm O_2/Ar for W09/W21(X3)
		10 sccm/ 30 sccm O_2/Ar for W25A(22)
	I Additional:	10 min O_2 gas flow at 20 sccm/20 sccm for
	M3 Material:	Titanium
	M3 Temp:	500°C

	M3 Dep Time:	
	M3 Gas Flow:	20 sccm/ 20 sccm O_2/Ar for W09/W21(X3) 10 sccm/ 30 sccm O_2/Ar for W25A(22)
Cleaning:	(ALL – 08/04/2009)	
	Solution(s):	Acetone/IPA/De-mineralized water rinse
	Post Process:	Nitrogen dry
	Soft Bake:	110°C for ~4 min
Spin-On Resist:	(ALL – 08/04/2009)	
	Resist Type:	AZ 5214 (Positive mode)
	Spinner:	Manual Spinner (Hood #9)
	Spin Speed:	2000 RPM
	Spin Time:	40 s
	Resist Amount:	½ test tube per wafer
	Soft Bake Temp:	110°C
	Soft Bake Time:	60 s
Photoalignment:	(ALL – 08/04/2009)	
	Aligner:	Karl Suss MA6 Aligner (New)
	Contact Type:	Lo Vac
	Al Gap:	40 um
	Exposure Time:	2.8 s
	Wattage/Chan:	~340 W / Channel 1
Development:	(ALL – 08/04/2009)	
	Solution:	AZ 300 MIF
	Develop Method:	Submersion with agitation
	Develop Time:	75-85 s
	Post Treatment:	Demineralized water rinse for ~40 s
	Inspection:	Overall, feature sizes came out well
Ashing:	(ALL – 08/04/2009)	
	Tool:	Metroline M4L Plasma Asher
	Recipe:	5214.descum.5min
UV Curing:	(ALL – 08/04/2009)	
	Tool:	Axcelis UV Photoresist Stabilizer
	Recipe:	RON_220C
Notes:	PR residue present on edges due to neglecting edge bead removal	
Ion Milling:	(W25A – 08/06/2009, W21 – 08/10/2009, W09 – 08/11/2009)	
	Tool:	4Wave Ion Beam Etch System
	Recipe:	
	End Point Recipe:	Hiden Program 7; dARL003.exp

Inspection: Over-etching occurred on all wafers due to miscalculated endpoint amplitude for platinum. This has been corrected.

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Appendix B. Measurement Settings for the Keithley 4200 SCS

Project Name: Metal-Insulator-Metal Diode Project (Component of Rectenna)
Experiment Name: Fabrication and electrical testing of Ti/TiO2/Pt MIM diode pillars (Trial Set 1)
Entry Type: Experimental Plan
Entry Page Span: 3 pages

Purpose of Experiment:

The purpose is to produce a first run of MIM diode devices based on a Ti/TiO2/Pt stack, and then acquire I-V characteristics of the diode structures in hopes of a very low turn-on voltage. The titanium and platinum metals were chosen for their large work function difference between the two metals, and the titanium dioxide was chosen due to the ability to grow a thin film of the insulator material on the titanium in a controlled environment. There is also evidence from simulations that the titanium dioxide might have a low barrier height compared to other insulating materials. This first run will make use of a low-temperature deposition and lift-off process. Future runs will be performed using a high-temperature deposition and ion milling process. I-V measurements will be performed on

General Order of Operations:

1. Fabricate MIM diodes using one of two processes
    a. Low-temperature deposition recipes in conjunction with a lift-off process
    b. High-temperature deposition recipes in conjunction with an ion milling process
2. Measurement of MIM diodes using a probe station and a DC parameter measurement system
    a. I-V sweeps between -0.2 mV and +0.2 mV
    b. I-V sweeps between -2.0 mV and +2.0 mV
3. Device thickness confirmation through profilometer measurements

Note: It should be noted that for the higher applied voltages, the current of the devices will most likely be outside of the measurable limits of the measurement tool being used (Keithley 4200 SCS).

General Sample Specifications:

Substrate:	Silicon 4-in wafer with varying parameters (thickness, dopants, oxides)
Metal Underlayer:	Either a uniform blanket gold film, or no metal underlayer present
MIM Stack:	Titanium/Titanium Dioxide/Platinum stack of varying thicknesses

Independent Variables:

1. MIM stack deposition thicknesses (for Titanium, Platinum and Titanium Dioxide)
2. MIM stack deposition temperature (50 °C vs. 500 °C)
3. Patterning method (lift-off vs. ion milling)
4. Metal underlayer (gold vs. no gold)

Measurement Test Equipment:

- Keithley 4200 Semiconductor Characterization System (with pre-amps)
- Micromanipulator standard probe station

Electrical Measurement Test Settings:

I-V Sweep for two-terminal diode device (-0.2mV to 0.2mV)

- Cathode (SMU2)
    - Forcing Function = Voltage Sweep (Master ON); Sweep Type = Linear (Dual OFF)
    - Power On Delay = 0s; Pulse Mode = OFF
    - Start = -0.0002V; Stop = 0.0002V; Step = 2e-6V; Data Points = 201; Src Range = Best Fixed; Compliance = 0.011A;
    - Measuring Options = Current ON (100mA); Voltage ON (Measured)
- Anode (SMU1)
    - Forcing Function = Voltage Bias
    - Power On Delay = 0s
    - Level = 0V; Src Range = Best Fixed; Compliance = 0.1A
    - Measuring Options = Current ON (100mA); Voltage ON (Measured)
- Timing
    - Speed = Normal
    - Sweeping Mode = ON; Sweep Delay = 0s; Hold Time = 0s
    - SMU Power On Sequence = Anode, Cathode
    - Timestamp Enabled = ON; Disable outputs at completion = ON

I-V Sweep for two-terminal diode device (-2mV to 2mV)

- Cathode (SMU2)
    - Forcing Function = Voltage Sweep (Master ON); Sweep Type = Linear (Dual OFF)
    - Power On Delay = 0s; Pulse Mode = OFF
    - Start = -0.002V; Stop = 0.002V; Step = 2e-5V; Data Points = 201; Src Range = Best Fixed; Compliance = 0.011A;
    - Measuring Options = Current ON (100mA); Voltage ON (Measured)
- Anode (SMU1)
    - Forcing Function = Voltage Bias
    - Power On Delay = 0s
    - Level = 0V; Src Range = Best Fixed; Compliance = 0.1A
    - Measuring Options = Current ON (100mA); Voltage ON (Measured)
- Timing
    - Speed = Normal
    - Sweeping Mode = ON; Sweep Delay = 0s; Hold Time = 0s
    - SMU Power On Sequence = Anode, Cathode
    - Timestamp Enabled = ON; Disable outputs at completion = ON

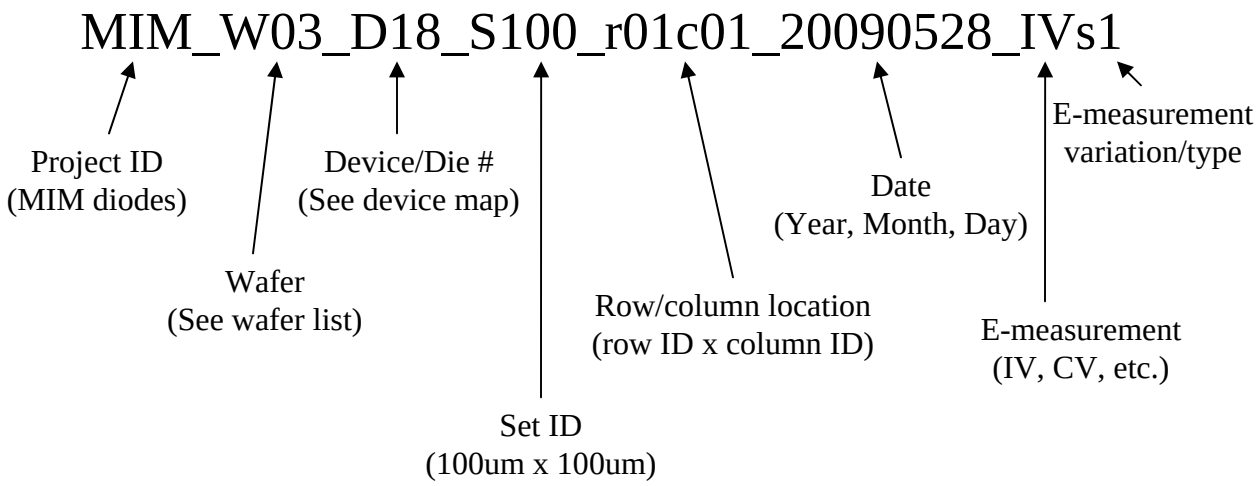
MIM Diode Experimental Data Naming Conventions:

Data will initially save to: Keithley 4200 SCS (Nanoelectronics Lab Tool)
C:\Data\MIM_xxxx…

Data will be copied to: Matthew Chin's Share Drive (M:\)
M:\Data_MIM\MIM_2009_xx_yy\
Where xx is the month, and yy is the day

File Type: Microsoft Excel File (".xls")

Example Name: MIM_W03_D18_S100_r01c01_20090528_IVs1



Electrical measurement variation numbers:

ID	Gold (Au) probe	Platinum (Pt) probe	Voltage Sweep Range	Data Points
S1	SMU1 (L)	SMU2 (R)	-2.0 mV to +2.0 mV	201
S2	SMU1 (L)	SMU2 (R)	-0.2 mV to +0.2 mV	201
S3	SMU2 (R)	SMU1 (L)	-2.0 mV to +2.0 mV	201
S4	SMU2 (R)	SMU1 (L)	-0.2 mV to +0.2 mV	201

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Appendix C. Design of Experiment for TiO_2 Development

Project Name: Metal-Insulator-Metal Diode
Experiment Name: Titanium Dioxide Recipe and Process Development
Entry Type: Experimental Plan
Entry Page Span: 3 pages

Description of Experiment:

After reviewing the data of the first two MIM diode fabrication trials, it appears that changes in the process flow need to take place. Evidence from the data suggests that there are either a lot of pinholes present in the current titanium dioxide layer being created, or a titanium dioxide layer is not being formed during the process. The same ohmic, linear slopes of the I-V characteristics were the same between the supposed 40 Å-thick grown titanium dioxide layer and the 0 Å-thick non-layer. A discussion with Ron confirmed that the recipes available on the CLC 200 Clusterline deposition tool were only experimental ones that did not provide uniform coverage of the surface.

It has been determined that a process to get a uniform, thin titanium dioxide layer must be developed for the CLC 200 Clusterline tool. Tunneling is very dependent on this layer, so it is essential that the titanium dioxide can be reliably produced at the specified thickness. To accomplish this, a "design of experiment" will be performed to determine the optimal parameter settings to produce a uniform layer of titanium dioxide for thicknesses in the sub-10 angstrom range. Rob Mamazza from Unaxis (company that developed the CLC 200 Clusterline tool) will provide assistance in terms of direction for recipe development and creating the design of experiment set.

General Order of Operations (Developed with the help of Rob Mamazza):

1. Develop a design of experiment that with the 3 most critical parameters
    a. Oxygen Concentration with a low of 38 sccm/02 sccm Ar/O_2, a mid of 29 sccm/11 sccm Ar/O_2, and a high of 20 sccm/20 sccm Ar/O_2
    b. Substrate Temperature with a low of 300 °C, a mid of 400 °C, and a high of 500 °C
    c. Time with a low of 96 s (associated with ~5 nm of TiO_2), a mid of 961 s (associated with ~50 nm of TiO_2), and a high of 1923 s (associated with 100 nm of TiO_2)
2. Create recipes on the Clusterline tool for each experiment in the design
3. Perform a limited test run with a few critical variations based on the original recipes
    a. Lock the temperature at 500°C and hold the gas ratio at 20 sccm/20 sccm Ar/O2 while changing only the time for the low, mid, and high values specified in 1c above
4. Determine a method to confirm film uniformity and thickness
    a. Although there are a few major metrology techniques to measure the thickness of a known material, the composition of the titanium dioxide being grown/sputtered is not known, so many of the standard methods may not work
    b. Device performance could potentially be used to determine the thickness. At the

very least, it would tell the point where the oxide is considered too thick

Note: Since metal is being deposited as well, there might be a chance that not all of the metal reacts, leaving conductive traces in the oxide film – this must be corrected by fully oxidizing all remaining Ti.

General Sample Specifications:

Substrate:	Silicon 4-in wafer with varying parameters (thickness, dopants, oxides)
Metal Underlayer:	Platinum using a standard recipe that has a thickness of ~1000 Å
Oxide Layer:	Titanium dioxide at varying thicknesses
Metal Overlayer:	This will not be laid down initially

Independent Variables:

1. Oxygen Concentration or Argon/Oxygen Ratio
2. Substrate Temperature
3. Time

Deposition Tool Sets

- Unaxis Clusterline CLC 200 Sputtering System

Metrology Tool Sets

- Physical Profilometry
- Optical Profilometry
- Ellipsometry
- Electrical Measurements

Design of Experiments List:

Experiment ID	Temperature	Gas Ratio (Ar/O_2)	Time	Fab Start Date
W01	300 C	36 sccm / 04 sccm	0096 s	
W02	300 C	36 sccm / 04 sccm	0961 s	
W03	300 C	36 sccm / 04 sccm	1923 s	
W04	300 C	30 sccm / 10 sccm	0096 s	
W05	300 C	30 sccm / 10 sccm	0961 s	
W06	300 C	30 sccm / 10 sccm	1923 s	
W07	300 C	20 sccm / 20 sccm	0096 s	July 23, 2009
W08	300 C	20 sccm / 20 sccm	0961 s	July 22, 2009
W09	300 C	20 sccm / 20 sccm	1923 s	July 23, 2009
W10	400 C	36 sccm / 04 sccm	0096 s	
W11	400 C	36 sccm / 04 sccm	0961 s	
W12	400 C	36 sccm / 04 sccm	1923 s	
W13	400 C	30 sccm / 10 sccm	0096 s	
W14	400 C	30 sccm / 10 sccm	0961 s	
W15	400 C	30 sccm / 10 sccm	1923 s	
W16	400 C	20 sccm / 20 sccm	0096 s	
W17	400 C	20 sccm / 20 sccm	0961 s	
W18	400 C	20 sccm / 20 sccm	1923 s	
W19	500 C	36 sccm / 04 sccm	0096 s	
W20	500 C	36 sccm / 04 sccm	0961 s	
W21	500 C	36 sccm / 04 sccm	1923 s	
W22 (W25A)	500 C	30 sccm / 10 sccm	0096 s	July 21, 2009
W23 (W26A)	500 C	30 sccm / 10 sccm	0961 s	July 21, 2009
W24 (W27A)	500 C	30 sccm / 10 sccm	1923 s	July 22, 2009
W25	500 C	20 sccm / 20 sccm	0096 s	July 24, 2009
W26	500 C	20 sccm / 20 sccm	0961 s	July 24, 2009
W27	500 C	20 sccm / 20 sccm	1923 s	July 24, 2009

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